

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

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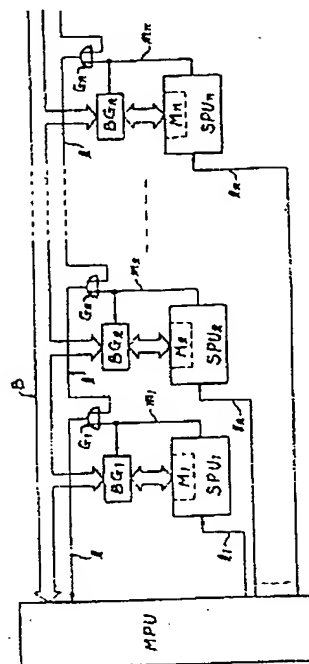
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TITLE : COMMUNICATION CONTROL SYSTEM  
BETWEEN PROCESSORS



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ABSTRACT : PURPOSE: To attain direct access to main control processor for the communication area of the memory of a sub ordinate control processor by sending a request for communication from the main control processor and placing the subordinate control processor in a temporary stop state.

CONSTITUTION: The main control processor MPU sends communication request information to the subordinate control processor SPU<sub>1</sub>. The subordinate control processor SPU<sub>1</sub> sends communication ready information to an information line m<sub>1</sub> and holds itself in a temporary suspending stop state. The communication ready information of the information line m<sub>1</sub> opens a bus gate BG<sub>1</sub> corresponding to the subordinate control processor SPU<sub>1</sub>. Consequently, the main control processor MPU attains direct access to the memory M<sub>1</sub> of the subordinate control processor SPU<sub>1</sub>. When the communication ready information of the information line m<sub>1</sub> is ceased, the bus gate BG<sub>1</sub> is closed and the communication ready information of the information line I<sub>1</sub> is also ceased. Thus, communication control over all subordinate control processors SPU<sub>1</sub>~SPU<sub>n</sub> is performed.

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